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(54) **A low-absorption circuit device for controlling a power transistor into the on state.**

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Descripti n

This inv nti n relates to a low-abs rption circuit device for controlling a power transistor, in particular a D MOS transistor having conventional gate, drain, and source electrodes and being adapted for driving electrical loads by changing over from an off state to an on state in which a predetermined voltage value appears on the gate electrode.

As is known, D MOS n-channel power transistors are currently extensively used as high-side drivers in bridge circuits to drive inductive loads.

Such bridge circuits have to be supplied electrically, in addition to a supply voltage Vcc, with a higher voltage Vcp than the supply voltage which is applied to the gate electrode on such power transistors in use as high-side drivers. This additional voltage value is specially needed under those conditions of operation when a power transistor delivers maximum current with a minimum voltage drop between its drain and source electrodes.

Furthermore, that voltage value is supplied to that transistor in the bridge circuit by means of a purposely provided turn-on circuit.

The voltage Vcp may be supplied by a feeder; however, where such a feeder is not available, said voltage value would be generated at one end of a so-called bootstrap capacitor Cp arranged to function as a charge storage. To that one end of the capacitor Cp, each turn-on circuit for each power transistor employed as a high-side driver in the bridge circuit is connected. The capacitor Cp is re-charged periodically by means of a re-charge circuit so as to keep the voltage value Vcp unchanged.

A circuit device according to the preamble portion of the independent claim 1 is known from document "Siemens Components XIX (1984) No.4, pages 169-170, H.RABL: Operation of SIPMOS Transistors with Grounded Loads".

It is a current practice in the art to use, for each power transistor, a respective turn-on circuit which is input connected and powered directly from said capacitor, to which a plurality of power transistors from several possible bridge circuits may be connected.

That prior approach has drawbacks deriving from that, on changing over the power transistor from the off state to the on state, the achievement of a correct supply voltage value on the gates of such transistors is entirely demanded to said capacitor, which will exhibit a high absorption of charges. As a result, the use of large size capacitors and of a re-charge circuit of correspondingly large size becomes mandatory.

The technical problem that underlies this invention is to provide a circuit device for controlling power transistors to b coming conductive, which has such structural and performance charact ristics as to minimize the absorpti n of charges by a capacitive supply source during the change-over phase from the off state to the on state, thus bviating th cited drawbacks with which the prior art is b set.

This problem is solv d by a circuit device as specified in the independent claim 1.

The features and advantages of the device according to the invention will be more clearly understood by having reference to the following detailed d - scription of an embodiment thereof, to be taken by way of illustration in conjunction with the accompanying drawing.

The drawing single figure shows in schematic form a circuit device according to this invention.

With reference to the drawing view, the numeral 1 generally and schematically designates a low-absorption circuit device for controlling a power transistor 2 into the on state. The transistor 2 is, in this non-limitative embodiment, a D MOS n-channel power transistor type connected, together with other transistors 3 of the same type and functioning as a high-side driver, in a bridge circuit 4 for driving inductiv electrical loads 5.

The transistor 2 is conventionally provided with gate G, drain D, and source S electrodes. The drain D is connected to one pole of a voltage supply Vcc, and a diode D8 is connected between the source S and the gate G.

The device 1 comprises a first turn-on circuit 6 having a transistor pair, respectively designated M1 and M2, of the p-channel MOS type with respective gate electrodes G1 and G2 interconnected and respective source electrodes S1 and S2 connected as inputs to the voltage supply Vcc pole.

The gate G1 and drain D1 of the transistor M1 are shorted to each other, the output of the turn-on circuit 6 being formed by the drain electrode D2 of the transistor M2 connected to the gate G of the power transistor 2 via a diode D5.

In accordance with this invention, a second turn-on circuit 7 is provided which also includes a transistor pair M3,M4 of the p-channel MOS type with respective gates G3 and G4 connected to each other.

The respective source electrodes S3 and S4 of those transistors M3 and M4 are connected to a second pole of the voltage supply Vcp present at one end of a so-called bootstrap capacitor Cp.

The gate G3 and drain D3 of the transistor M3 are shorted to each other, whilst the drain D4, forming the output of the second turn-on circuit 7, is connected directly to the gate G of the power transistor 2. That gate G is also connected to a turn-off circuit 8.

The construction of the circuit device 1 is completed by a comparator 9 comprising a transistor DM1 of the n-channel MOS type having as a first input thereof th gate electrode GM1 conn cted to ground, via a current source A, and to the supply pol Vcc via a Z ner diode DZ across which a voltag drop Vz appears. A resistor R1 interconnects the gate GM1 and source SM1 of the transistor DM1, whilst the drain P1

is connected with output functions for the comparator 9 to the drain D1 of the transistor M1 in the turn-on circuit 6.

The comparator 9 comprises a second transistor DM2 of the n-channel D MOS type having its drain P2 connected as a second output to the drain D3 of the transistor M3 in the second turn-on circuit 7. The transistor DM2 has its gate electrode GM2 connected as a second input to the gate G of the power transistor 2 via two serially connected diodes D6 and D7; in addition, the gate GM2 and source SM2 are connected to each other via a resistor R2.

The sources SM1 and SM2 of the transistors in the comparator 9 are connected together and to ground via a switch 10 and current source A1 connected in series.

The operation of the device 1 according to the invention will be described herein below with reference to an initial condition whereby the power transistor 2 is in an off state, with the gate electrode at zero Volts, and the switch 10 is on.

Under that condition, on the gate GM1 of the transistor DM1 there appears a voltage Vr resulting from the difference of the supply voltage Vcc less the voltage drop Vz across the Zener diode DZ.

This transistor DM1 is therefore conductive, and will activate the first turn-on circuit 6 to, in turn, drive the transistor 2 into the on state.

The circuit 6 will supply the gate G of the transistor 2 up to a voltage value given by the difference of the supply voltage Vcc minus the combined voltage drops between the source and the drain of the transistor M2 and across the diode D5.

To further increase the voltage on the gate G, the second turn-on circuit 7 cuts in at this point, being activated by the comparator 9 based on a comparison of the voltage values between its inputs GM1 and GM2. In particular, the circuit 7 becomes operative upon the voltage on the gate G, and hence, on the input GM2 exceeding a value given by the sum of the voltage Vr plus the voltage drops across the diodes D6 and D7. The latter voltage value may be adjusted by suitably selecting the Zener diode DZ, the objective being that of balancing the conflicting needs to minimize the absoprtion of charges by the capacitor CP and at the same time avoid slow-downs in the change-over phase due to saturation of the transistor M2.

The moment the circuit 7 is activated, all the current from the current source A1 will flow through the transistor DM2 and put the first circuit 6 out of conduction which is also cut off by the provision of the diode D5.

At the end of each change-over phase, the resistors R1 and R2 will restore the comparator 9 to a balance condition.

By using identical transistors DM1 and DM2, M1 and M3, M2 and M4 for the respective circuits 6, 7, 9, it becomes possible to obtain a continuous up curve for the gate G voltage, and a consequently similar waveform for the output voltage to be supplied to the inductive load 5.

The device of this invention affords a major advantage in that it can minimize the absorption of charges by the capacitor Cp, thus enabling the size of that capacitor to be reduced. This advantage also reflects in the possibility to reduce the size of the recharge circuit provided to maintain the reference voltage value across said capacitor, or contingent on requirements, in the possibility to drive a number of bridge circuits at higher change-over rates.

Claims

1. A circuit device for turning-on a power MOS transistor (2) connected in a high-side driver configuration between a first (VCC) and a second pol of a main voltage supply through an electrical load, said device comprising means for connecting the gate of the power MOS transistor to a capacitive voltage supply which provides a voltag (VCP) higher than the voltage of the main voltage supply, characterized in that it comprises

   a first turn-on circuit (6) for selectively connecting the gate of the power MOS transistor (2) to the first pole (VCC) of the main voltage supply,

   a second turn-on circuit (7) for selectively enabling said means for connecting the gate of the power MOS transistor (2) to said capacitiv voltage supply (VCP) and

   a comparator (9) having a first input (GM1) connected to a source of a predetermined reference voltage (VR), a second input (GM2) connected to the gate (G) of the power MOS transistor (2) and first (P1) and second (P2) complementary outputs connected to the first (6) and second (7) turn-on circuits, respectively, and adapted to selectively actuate the first (6) or second (7) turn-on circuit if the voltage at its second input (GM2) is lower or higher than said reference voltage (VR), respectively.

2. A device according to Claim 1, characterized in that said first turn-on circuit (6) comprises a pair of MOS transistors (M1,M2) having respective gate electrodes (G1,G2) connected to each other and respective source electrodes connected to said first pole (Vcc) of said main voltage supply, the gate (G1) and drain (D1) electrodes of one transistor (M1) being connect d to each other and t th first output (P1) of the comparator (9), the drain el ctrode (D2) of the other transistor (M2) being connected to th gat (G) f said power MOS transistor (2) as th output of the circuit

(6).

3. A device according to Claim 1, characterized in that said second turn-on circuit (7) comprises a pair of MOS transistors (M3,M4) having respective gate electrodes (G3,G4) connected to each other and respective source electrodes (S3,S4) connected to said capacitive voltage supply (Vcp), the gate (G3) and drain (D3) electrodes of one transistor (M3) being connected to each other and to the second output (P2) of the comparator (9), and the drain electrode (D4) of the other transistor (M4) being connected, as the output of the circuit (7), to the gate (G) of said power MOS transistor (2).

4. A device according to Claim 1, characterized in that said comparator (9) comprises a pair of MOS transistors (DM1,DM2) having respective source electrodes (SM1,SM2) connected to each other, one transistor (DM1) having its gate electrode (GM1) connected as the first input to said reference voltage (Vr) and the other transistor (DM2) having its gate electrode (GM2) connected to the gate (G) of said power MOS transistor (2).

5. A device according to Claim 4, characterized in that said source electrodes (SM1,SM2) of said MOS transistor pair are connected to the second pole of the main voltage supply via a serially connected switch (10) and current source (A1).

Patentansprüche

1. Ein Schaltungsgerät zum Einschalten eines Leistungs-MOS-Transistors (2), der in einer Hochseiten-Treiberkonfiguration zwischen einem ersten (VCC) und einem zweiten Pol einer Hauptspannungsversorgung über eine elektrische Last verschaltet ist, wobei das Gerät eine Einrichtung zum Verbinden des Gate des Leistungs-MOS-Transistors mit einer kapazitiven Spannungsversorgung umfaßt, die eine Spannung (VCP) bereitstellt, die größer ist als die Spannung der Hauptspannungsversorgung, dadurch gekennzeichnet, daß es folgende Merkmale umfaßt:
eine erste Einschaltschaltung (6) zum auswahlmäßigen Verbinden des Gate des Leistungs-MOS-Transistors (2) mit dem ersten Pol (VCC) der Hauptspannungsversorgung,
eine zweite Einschaltschaltung (7) zum auswahlmäßigen Aktivier n der Einrichtung zum Verbind n des Gat d s Leistungs-MOS-Transistors (2) mit der kapazitiven Spannungsversorgung (VCP), und
einen Komparator (9) mit einem ersten Eingang (GM1), der mit einer Quelle einer vorbestimmten R ferenzspannung (VR) verbunden ist, einem zweiten Eingang (GM2), der mit dem Gate (G) des Leistungs-MOS-Transistors (2) verbunden ist, und einem ersten (P1) und einem zweiten (P2) komplementären Ausgang, der mit der ersten (6) bzw. mit der zweiten (7) Einschaltschaltung verbunden ist und angepaßt ist, um auswahlmäßig die erste (6) oder die zweite (7) Einschaltschaltung zu betätigen, wenn die Spannung an seinem zweiten Eingang (GM2) niedriger bzw. höher ist als die Referenzspannung (VR).

2. Ein Gerät nach Anspruch 1, dadurch gekennzeichnet,
daß die erste Einschaltschaltung (6) ein Paar von MOS-Transistoren (M1, M2) aufweist, deren jeweilige Gate-Elektroden (G1, G2) miteinander verbunden sind, und deren jeweilige Source-Elektroden mit dem ersten Pol (VCC) der Hauptspannungsversorgung verbunden sind, wobei die Gate- (G1) und die Drain- (D1) Elektrode des einen Transistors (M1) miteinander und mit dem ersten Ausgang (P1) des Komparators (9) verbunden sind, wobei die Drain-Elektrode (D2) des anderen Transistors (M2) mit dem Gate (G) d s Leistungs-MOS-Transistors (2) als Ausgang d r Schaltung (6) verbunden ist.

3. Ein Gerät gemäß Anspruch 1, dadurch gekennzeichnet,
daß die zweite Einschaltschaltung (7) ein Paar von MOS-Transistoren (M3, M4) umfaßt, deren jeweilige Gate-Elektroden (G3, G4) miteinander verbunden sind, und deren jeweilige Source-Elektroden (S3, S4) mit der kapazitiven Spannungsversorgung (VCP) verbunden sind, wobei die Gate- (G3) und die Drain- (D3) Elektrode d s einen Transistors (M3) miteinander und mit d m zweiten Ausgang (P2) des Komparators (9) v rbunden sind, und wobei die Drain-Elektrode (D4) des anderen Transistors (M4) mit dem Gate (G) des Leistungs-MOS-Transistors (2) als der Ausgang der Schaltung (7) verbunden ist.

4. Ein Gerät nach Anspruch 1, dadurch gekennzeichnet,
daß der Komparator (9) ein Paar von MOS-Transistoren (DM1, DM2) umfaßt, deren jeweilige Source-Elektroden (SM1, SM2) miteinander verbunden sind, wobei die Gate-Elektrode (GM1) des einen Transistors (DM1) als der erste Eingang mit der Referenzspannung (Vr) verbunden ist, und di Gate-Elektrode (GM2) des anderen Transistors (DM2) mit d m Gate (G) des Leistungs-MOS-Transistors (2) verbunden ist.

5. Ein Gerät gemäß Anspruch 4, dadurch g kenn-

zeichnet,
daß die Source-Elektroden (SM1, SM2) des MOS-Transistorpaares über einen Schalter (10) und eine Stromquelle (A1), die seriell verschaltet sind, mit dem zweiten Pol der Hauptspannungsversorgung verbunden sind.

Revendications

1. Dispositif à circuit pour la mise en conduction d'un transistor MOS (2) de puissance connecté dans une configuration d'attaque à côté à potentiel haut entre un premier pôle (VCC) et un second pôle d'une alimentation principale en tension à travers une charge électrique, ledit dispositif comportant des moyens pour connecter la grille du transistor MOS de puissance à une alimentation en tension capacitive qui produit une tension (VCP) supérieure à la tension de l'alimentation en tension principale, caractérisé en ce qu'il comporte

un premier circuit (6) de mise en conduction pour connecter sélectivement la grille du transistor MOS (2) de puissance au premier pôle (VCC) d'alimentation en tension principale,

un second circuit (7) de mise en conduction pour valider sélectivement lesdits moyens destinés à connecter la grille du transistor MOS (2) de puissance à ladite alimentation en tension capacitive (VCP), et

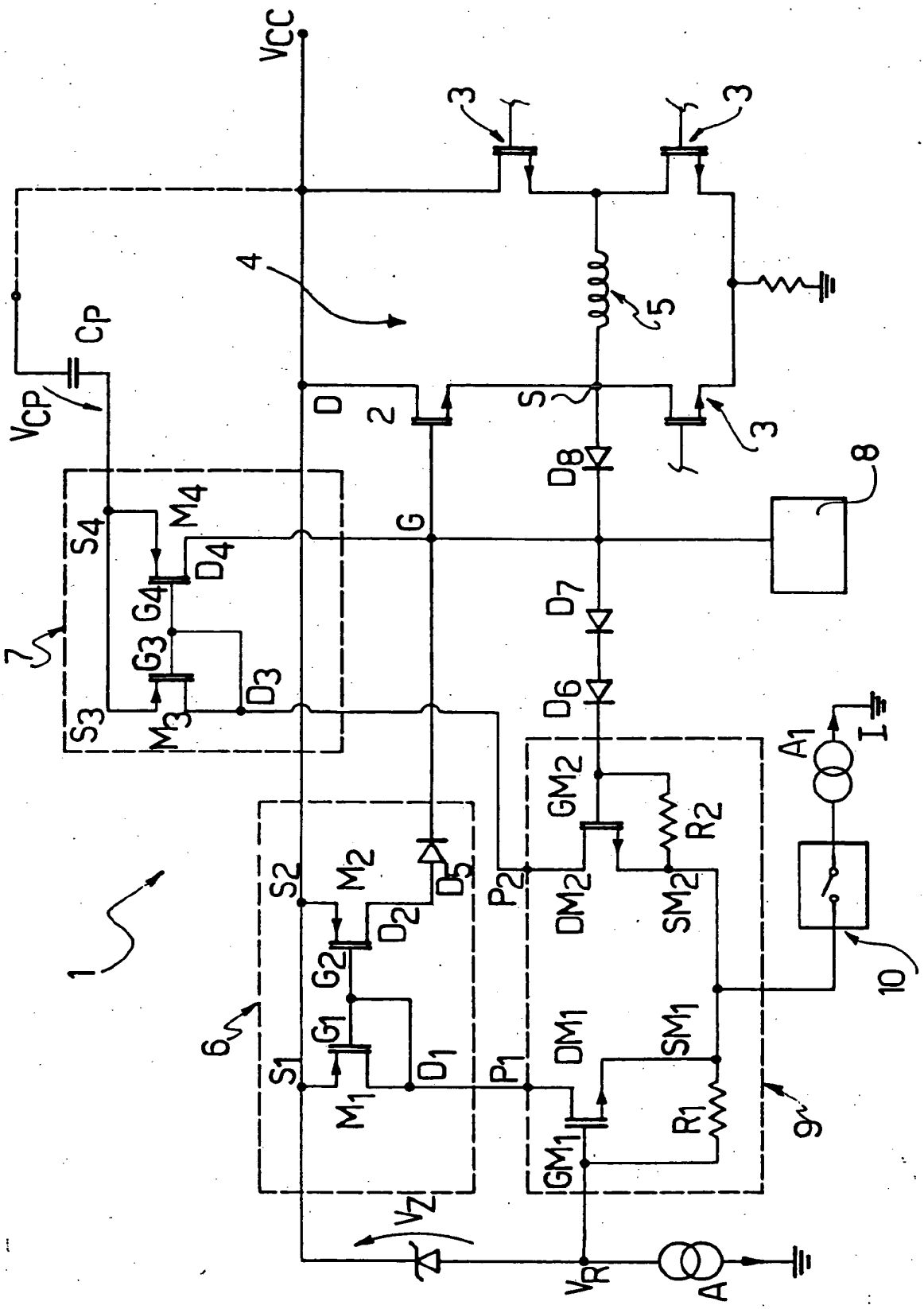
un comparateur (9) ayant une première entrée (GM1) connectée à une source d'une tension de référence prédéterminée (VR), une seconde entrée (GM2) connectée à la grille (G) du transistor MOS (2) de puissance et des première (P1) et seconde (P2) sorties complémentaires connectées au premier (6) et second (7) circuits de mise en conduction, respectivement, et destinées à actionner sélectivement le premier (6) ou second (7) circuit de mise en conduction si la tension à sa seconde entrée (GM2) est inférieure ou supérieure à ladite tension de référence (VR), respectivement.

2. Dispositif selon la revendication 1, caractérisé en ce que ledit premier circuit (6) de mise en conduction comporte deux transistors MOS (M1, M2) ayant des électrodes de grille respectives (G1, G2) connectées entre elles et des électrodes de source respectives connectées audit premier pôle (VCC) de ladite alimentation en tension principale, les électrodes de grille (G1) et de drain (D1) d'un transistor (M1) étant connectés entre elles et à la première sortie (P1) du comparateur (9), l'électrode de drain (D2) de l'autre transistor (M2) étant connectée à la grille (G) dudit transistor MOS (2) de puissance en tant que sortie du circuit (6).

3. Dispositif selon la revendication 1, caractérisé en ce que ledit second circuit (7) de mise en conduction comporte deux transistors MOS (M3, M4) ayant des électrodes de grille respectives (G3, G4) connectées entre elles et des électrodes de source respectives (S3, S4) connectées à ladite alimentation en tension capacitive (Vcp), les électrodes de grille (G3) et de drain (D3) d'un transistor (M3) étant connectées entre elles et à la seconde sortie (P2) du comparateur (9), et l'électrode de drain (D4) de l'autre transistor (M4) étant connectée, en tant que sortie du circuit (7), à la grille (G) dudit transistor MOS (2) de puissance.

4. Dispositif selon la revendication 1, caractérisé en ce que ledit comparateur (9) comporte deux transistors MOS (DM1, DM2) ayant des électrodes de source respectives (SM1, SM2) connectées entre elles, un transistor (DM1) ayant son électrode de grille (GM1) connectée en tant que première entrée à ladite tension de référence (Vr) et l'autre transistor (DM2) ayant son électrode de grille (GM2) connectée à la grille (G) dudit transistor MOS (2) de puissance.

5. Dispositif selon la revendication 4, caractérisé en ce que lesdites électrodes de source (SM1, SM2) de ladite paire de transistors MOS sont connectées au second pôle d'alimentation en tension principale par l'intermédiaire d'un interrupteur (10) connecté en série et d'une source (A1) de courant.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